AYDIN ADNAN MENDERES UNIVERSITY
EE207 – LOGIC DESIGN LABORATORY (18/19)

SLYYABUS

Date	Experiment
08.10.2018	**EXP #1: DIGITAL LOGIC GATES**
15.10.2018	**EXP #2: SIMPLIFICATION OF BOOLEAN FUNCTIONS**
22.10.2018	**EXP #3: COMBINATIONAL CIRCUITS**
29.10.2018	**Holiday**
05.11.2018	**EXP #4: COMBINATIONAL CIRCUITS**
12.11.2018	**Midterm Exam**
19.11.2018	**Midterm Exam**
26.11.2018	**EXP #5: IMPLEMENTATION OF FULL ADDER WITH TWO HALF ADDERS AND AN OR GATE**
03.12.2018	**EXP #6: SEVEN SEGMENT DISPLAY**
10.12.2018	**EXP #7: COMBINATIONAL LOGIC USING MULTIPLEXERS**
17.12.2018	**EXP #8: LATCHES**
24.12.2018	**EXP #9: JK FLIP-FLOPS**
31.12.2018	**Make up**
07.01.2020	**Written & Practical Exam**