Arithmetic and Logic Instructions

Arithmetic instructions operate on whole numbers only and support addition, subtraction, multiplication and division.

Addition

ADD A, #66H ; add the hex number 66 to the accumulator A

ADD A, 66H ; add to accumulator A the contents of RAM address 0066H

Since four addressing modes are possible, the ADD A instruction can be written in different ways:

ADD A, 7PH (direct addressing)

ADD A, @R0 (indirect addressing)

ADD A, R7 (register addressing)

ADD A, #35H (immediate addressing)

All arithmetic instructions execute one machine cycle except the INC DPTR instruction (two machine cycles) and the MUL AB and DIV AB instructions (four machine cycles). (Note that one machine cycle takes 1 μs if the 8051 is operating from a 12 MHz clock.)

Accumulator A is an SFR; it is an 8-bit register and its RAM address is 00E0H. A large number of instructions use accumulator A, but not all.

INC 66H ; increment (add 1) the contents of address 0066H

Example 2.1

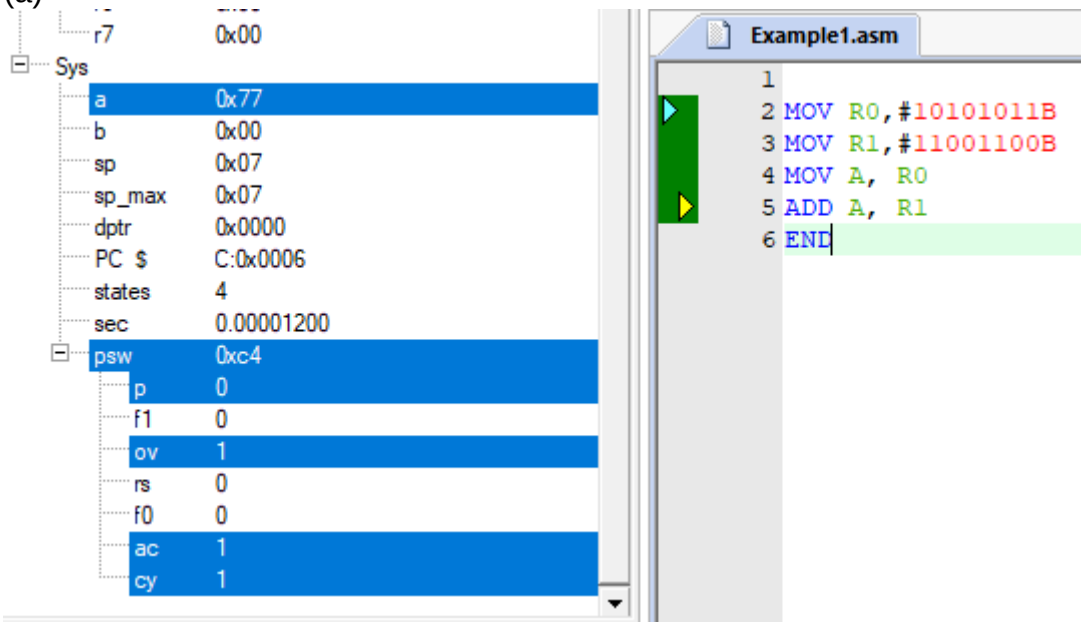
R0 contains 10101011 and R1 contains 11001100, and the PSW contains 00H. (a) What is the hexadecimal content of the accumulator and the PSW after execution of the following instruction?

```
MOV  R0,#10101011B
MOV  R1,#11001100B
MOV A, R0
ADD  A,  R1
END
```

(b) What is the content of the accumulator in decimal after execution of this instruction?

Solution

(a)



(b) 77H=7*16+7=119

Example 2.2

Suppose the 8051 did not have an instruction to directly increment an internal RAM location. How could this operation be achieved?

Solution

MOVE A,

direct INC A

MOV direct, A

Exercise 2.1

Is there any difference between the following two instructions?

A) INC A B) ADD A, #1

Subtraction

SUBB A, #66H ; subtract hex66 from the contents of A

The extra B in the instruction implies Borrow. If the contents of A are less than the number being subtracted then bit 7 of the program status word (PSW) SFR will be set.

DEC A ; decrement A by 1, put result into A

Exercise 2.2

Is there any difference between the following two instructions?

(1) DEC A (2) SUBB A,#1

Example 2.3

Illustrate an instruction sequence to subtract the content of R6 from R7 and leave the result in R7.

Solution

```
MOV A, R7
CLR C          ; clears the carry flag in the program status word
SUBB A, R6
MOV R7, A
```

Discussion

For both addition and subtraction, the accumulator holds one of the values for the operation. So, the first instruction above moves one of the bytes to the accumulator to prepare for the operation. The second instruction clears the carry flag in the program status word. This is required because the only form of the subtract instruction is SUBB—subtract with borrow.

The operation subtracts from the accumulator the source byte and the carry bit. For subtract operations, the carry bit serves as a "borrow" bit. If the state of the carry bit is unknown, it must be explicitly cleared using CLR C before executing SUBB. The third instruction performs the subtraction, leaving the result in the accumulator. The fourth instruction moves the result into R7.

The 8051 provides powerful addressing of its internal memory space. Any location can be incremented or decremented using direct addressing without going through the accumulator. For example, if internal RAM location 7FH contains 40H, then the instruction

INC 7FH

increments this value, leaving 41H in location 7FH.

Multiplication

MUL AB ; multiply the contents of A and B, put the answer in AB

A is the accumulator and B is another 8-bit SFR provided for use with the instructions multiply and divide. A and B are both 8-bit registers. The product of the multiplication process could be a 16-bit answer.

The MUL AB instruction multiplies the accumulator by the data in the B register and puts the 16-bit product into the concatenated[2] B (high-byte) and accumulator (low-byte) registers.

Example 2.4

A =135 decimal, B = 36 decimal. What would be the value in each register after executing the instruction MUL AB?

Solution

A x B =4860 = 0001 0010 1111 1100B = 12FCH

0001 0010 or 12H would be placed in A; 1111 1100 or FCH in B

Example 2.5

The accumulator contains 55H, the B register contains 22H, and the program status word contains 00H. What are the contents of these registers after execution of the following instruction?

MUL A B

Solution

ACC=4AH, B=0BH, PSW=05H

Discussion

You might be able to compute the answer using a calculator; otherwise begin by expressing the original values in decimal: ACC = 55H = 85_{10} and B = 22H = 34_{10}. The product is 85_{10} x 34_{10}
= $2{,}890_{10}$ = 0B4AH. The high byte (0BH) is placed in register B and the low byte (4AH) is placed in the accumulator. The P bit in the PSW is set to establish even parity with the accumulator. Since the result is greater than 255_{10}, the overflow flag is set, leaving the PSW containing 05H.

Example 2.6

The accumulator contains 1FH. What is the largest value that could be in register B such that the OV bit would not be set after executing the following instruction?

MUL AB

Solution

08H

Discussion

The accumulator contains 1FH = 31_{10}. The overflow flag is set following MUL if the product is greater than 255_{10}. The largest number that 31_{10} can be multiplied by without the product exceeding 255_{10} is 8_{10} = 08H. (Note 31_{10} x 8_{10} = 248_{10}, 31_{10} x 9_{10} = 279_{10}.)

Exercise 2.3

If A = 2FH and B = 02H, what would each register contain after execution of the instruction MUL AB?

Division

DIV AB ; divide A by B, put quotient in A and remainder in B

Example 2.7

A = 135, B = 36. What would be the value in each register after execution of the

instruction DIV AB?

Solution

Decimal values are assumed if the value quoted is not followed

by an H A/B =3; remainder 27 (27 = 1BH) : Hence 03H in A, 1BH

in B

Exercise 2.4

If A = 2FH and B = 02H, what would each register contain after the execution of the instruction DIV AB?

LOGIC OPERATIONS

The set of logic functions include:

ANL AND Logic

ORL OR Logic

XRL exclusive OR Logic

CPL Complement (i.e. switch to the opposite logic level)

RL Rotate Left (i.e. shift byte left)

RR Rotate Right (i.e. shift byte right)

SETB Set bit to logic 1

CLR Clear bit to logic 0

AND Operation

The ANL instruction is useful in forcing a particular bit in a register to logic 0 whilst not altering other bits. The technique is called masking.

Suppose accumulator contains EDH (1110 1101B),

1	1	1	0	1	1	0	1

bit 1 and bit 4 are at logic 0, the rest at logic 1.

ANL R1, #7FH ; 7FH = 0111 1111B, forces bit 7 to zero

1	1	1	0	1	1	0	1

AND

0	1	1	1	1	1	1	1

=

0	1	1	0	1	1	0	1

Exercise 2.5

If A = 2D, what would be the accumulator contents after execution of the instruction ANL A, #3BH?

OR Operation

Another aspect of masking is to use the ORL instruction to force a particular bit to logic 1, whilst not altering other bits.

Suppose accumulator contains A2H (1100 0010B),

1	0	1	0	0	0	1	0

bit 0, 2, 3, 4 and bit 5 are at logic 0, the rest at logic 1.

ANL A, #14H ; 14H = 0001 0100B, forces bit 2 and 4 to one

1	0	1	0	0	0	1	0

OR

0	0	0	1	0	1	0	0

=

1	0	1	1	0	1	1	0

A=B6H

The power control (PCON) SFR in the 8051 family, is not bit addressable and yet has a couple of bits that can send the microcontroller into idle mode[3] or power down mode, useful when the power source is a battery.

The contents of the PCON SFR are:

SMOD1	SMOD2		POF	GPF1	GPF2	PD	IDL

SMOD1 and 2 are used when setting the baud rate of the serial onboard peripheral. POF, GPF1 and GPF2 are indictor flag bits. IDL is the idle bit; when set to 1 the microcontroller core goes to sleep and becomes inactive. The on-chip RAM and SFRs retain their values. PD is the Power Down bit, which also retains the on-chip RAM and SFR values but saves the most power by stopping the oscillator clock.

ORL PCON,#02H ; enables Power

Down ORL PCON,#01H ; enables

Idle mode

Either mode can be terminated by an external interrupt signal.

[3] Idle mode: Bekleme modu

Exercise 2.6

If the contents of accumulator = 38H, what would the contents of that register be after execution of the following instruction?

ORL A, #9AH

CPL Complement Operation

The instructions described so far have operated on bytes (8 bits) but some instructions operate on bits and CPL is an example.

CPL P1^7 ; complement bit 7 on Port 1

Port 1 is one of the microcontroller's ports with 8

pins. Port 1

P1^7	P1^6	P1^5	P1^4	P1^3	P1^2	P1^1	P1^0
MSB						LSB	

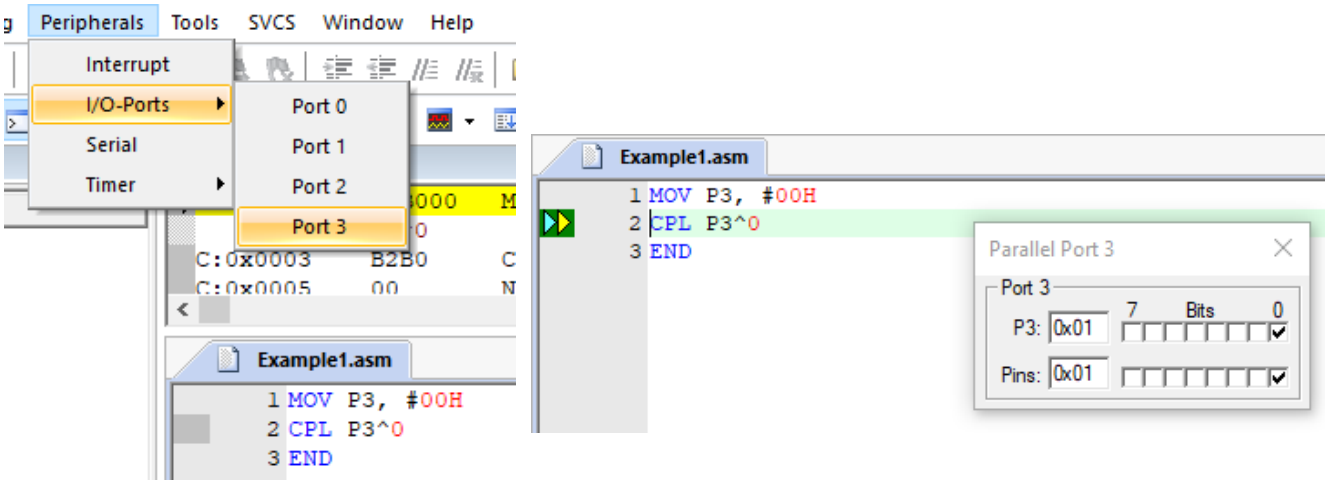
Example 2.8

What would be the value in port3 after executing the following instruction?

```
MOV P3, #00H
CPL P3^0
END
```

Solution

To open the Port screen, click on **Peripherals** -> **I/O-Ports** -> **Port 3**



P1=01H

Exercise 2.7

Is there any difference between the following two instructions? (MOV P2, #00H)

1) CLR P2^5 2) CPL P2^5

RL, rotate left one bit, RR, rotate right one bit operations

Suppose the accumulator A contents are 0000 0001B; this is 01H.

```
RL A        ; contents of A become 0000 0010B or 02H

RL A        ; 0000 0100B or 04H
RL A        ; 0000 1000B or 08H
```

RL three times has the effect of multiplying A by 2^3 i.e. by 8.

Suppose the accumulator A contents are 1000 0000B, or 128 decimal, then:

```
RR A ; contents of A become 0100 0000B which is 64 decimal
RR A ; A becomes 0010 0000B=32 decimal
RR A ; A becomes 0001 0000B=16 decimal
RR A ; A becomes 0000 1000B=8 decimal
```

RR four times has the same effect as dividing A by 2^4 i.e. 16. 128/16=8

Exercise 2.8

If the content of A is 128 and B is 2, what would the register

contents be after execution of the following instructions?

```
RR A
RL B
RR A
RR A
RL B
```

SETB set bit, CLR clear bit operations

This instruction operates on a bit, setting it to logic 1.

```
SETB P1^7    ; set bit 7 on Port 1 to logic 1
CLR P1^7     ; clears bit 7 on port 1 to zero
```