***Section and Group No:***

***Name:***

***Signature:***

## EXP #8: LATCHES

Components that will be ensured by the students: NOR, NAND and Inverter Gate.

***Objective(s):***

In this experiment, you will construct, test, and investigate the operation of various latches.

***Preliminary Work:***

**1)** The binary inputs given in the table below are supplied to the R and S inputs of the NOR SR latch given in Figure 1. Determine the states of the output Q and Q'.

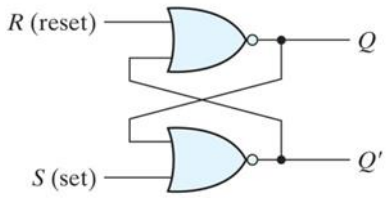



Figure 1

| S | R | Q | Q' |
|---|---|---|---|
| 0 | 1 | | |
| 0 | 0 | | |
| 1 | 0 | | |
| 0 | 0 | | |

Table 1: Truth Table

**2)** The binary inputs given in the table below are supplied to the En and D inputs of the D latch given in Figure 2. Determine the states of the output Q and Q'.

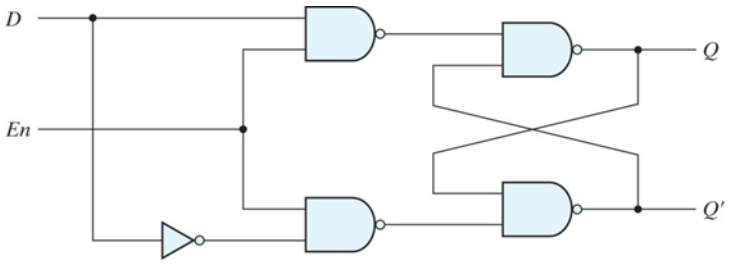



Figure 2

| En | D | Q | Q' |
|---|---|---|---|
| 0 | 1 | | |
| 1 | 1 | | |
| 0 | 0 | | |
| 1 | 0 | | |
| 0 | 1 | | |

Table 2: Truth Table

***Laboratory Work:***

**1)** Construct the circuits in your preliminary work. Fill the Table-3 and Table-4 and verify the truth tables with the given inputs.

**2)** Identify the each raw in the table with a statement (set, reset, undefined or no change).

| **S** | **R** | **Q** | **Q'** | **Statement** |
|---|---|---|---|---|
| 0 | 1 | | | |
| 0 | 0 | | | |
| 1 | 0 | | | |
| 0 | 0 | | | |

Table 3: SR Latch

| **En** | **D** | **Q** | **Q'** | **Statement** |
|---|---|---|---|---|
| 0 | 1 | | | |
| 1 | 1 | | | |
| 0 | 0 | | | |
| 1 | 0 | | | |
| 0 | 1 | | | |

Table 4: D Latch